REMARKS

This application has been reviewed in light of the Office Action dated December 10, 2004.

Claims 1-10 are now presented for examination. No amendment to the claims has been made. Claims 1 and 7 are independent. Favorable review is respectfully requested.

Claims 1-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Koch (U.S. Pat. No. 5,057,839). The applicants respectfully submit that independent claims 1 and 7 are patentably distinct from the cited art, for the following reasons.

The present invention, as defined in claim 1, is directed to a differential sampling circuit for generating a real differential input signal DC offset voltage. The circuit includes a first and a second switched-capacitor network. In particular, the first switched-capacitor network includes first, second and third capacitors and first through eighth switches. An embodiment of the invention is shown in Figure 6 of the specification, a copy of which is attached hereto as Exhibit A for convenience. In the switched-capacitor network 62' in this Figure, capacitors C1', C2' and C0' correspond to the first, second and third capacitors respectively; switches S1'-S8' correspond to the first through eighth switches respectively.

There are numerous distinct differences between the circuit of the present invention and the circuit of Koch (shown in Koch, Figure 1, a copy of which is attached as Exhibit B). Some examples of these differences are described below.

(1) The Examiner states that switch S1' of Koch is coupled to the positive input and the negative output of the opamp (as in the third switch S3' of the present invention). Figure 1 of Koch shows that switch S1' is not coupled to the negative output, but to capacitors C11', C13' and switch S3'. It is noteworthy that in the circuit of Koch, capacitor C1' connects the positive input and negative output at all times. In the present invention, by contrast, the positive input is shorted to the negative output when switch S3' is closed (see specification, Figures 5a and 5c).

(2) The Examiner states that capacitor C1' of Koch is coupled to the positive input and the second node (as in the second capacitor C2' of the present invention). Figure 1 of Koch shows that capacitor C1' is not coupled to the second node, but to the negative output of the

opamp. In this regard, it should be noted that the closest equivalent in Koch to the second node (23' in Figure 6 of the specification) is terminal T1 at the opposite end of switch S22' from the opamp.

(3) The Examiner states that switch S2' of Koch is coupled to the first node and the negative output (as in the sixth switch S6' of the present invention). Figure 1 of Koch shows that switch S2' is instead coupled to the positive input and capacitors C12', C14'. In Koch only switch S23' and capacitor C1' are connected to the negative output.

(4) The Examiner states that capacitor C12' of Koch is coupled to the positive input and the first node (as in the first capacitor C1' of the present invention). Figure 1 of Koch shows that capacitor C12' is not coupled to the positive input at all times, but only when switch S2' is closed (that is, phase "o" in Koch; see col. 5, lines 16-18). In this regard, it should be noted that the closest equivalent in Koch to the first node (22' in Figure 6 of the specification) lies between switch S8' and capacitor C12'.

(5) The Examiner states that capacitor C11' of Koch is coupled to the positive input and the third node (as in the third capacitor C0' of the present invention). Figure 1 of Koch shows that capacitor C11' is not coupled to the positive input at all times, but only when switch S1' is closed (that is, phase "e" in Koch; see col. 5, lines 13-16). In this regard, it should be noted that the closest equivalent in Koch to the third node (42' in Figure 6 of the specification) lies between switch S7' and capacitor C11'.

(6) The Examiner states that switch S7' of Koch is coupled to the first node and the third node (as in switch S8' in the present invention). Figure 1 of Koch shows that switch S7' is not coupled to the first node at all times, but only when switch S8' is closed (that is, phase "o" in Koch; see col. 5, lines 16-18).

The above remarks also apply to the second switched-capacitor circuit of the present invention, with reference to circuit 62" shown in Figure 6 of the specification.

More generally, Koch is concerned with a modulator with application to digital/analog converters. Koch is not understood to address the problem of differential input signal DC offset in high-speed communication lines, as in the present invention.

It is submitted that the arrangement of the circuit of Koch is clearly different from the circuit recited in Claim 1, so that the invention of Claim 1 is not anticipated by the cited reference.

Claim 7 is directed to a differential sampling circuit including a first capacitor and a second capacitor. It is a feature of the invention that a first terminal of each capacitor is connected to the input terminal of an opamp. Furthermore, it is a feature of the invention that the first capacitor and second capacitor are connected in parallel during a charge transfer operation in a portion of each system clock period.

The Examiner states that capacitors C12 and C11 of Koch meet the requirements of Claim 7. The applicants wish to point out that in the circuit of Koch, C11 and C12 are never connected to the opamp at the same time; C11 is connected when switch S1 is closed (phase "e"), while C12 is connected when switch S2 is closed (phase "o"). Furthermore, C11 and C12 are never connected in parallel. During phase "o", both terminals of C11 are connected to ground, while C12 is connected to terminal E and the opamp input. During phase "e", both terminals of C12 are connected to ground, while C11 is connected to terminal E and the opamp input. In this regard, Figure 2 of Koch and the discussion thereof at col. 4, line 63, to col. 5, line 6 are understood to teach that the signals in phases "e" and "o" may briefly be both L (low) but not both H (high). It therefore might be possible for switches associated with phases "e" and "o" to both be open, but not both closed.

In addition, Koch offers no teaching or suggestion regarding a charge transfer operation involving the two capacitors, and in particular does not disclose or suggest that such a charge transfer operation occur in a portion of each system clock period.

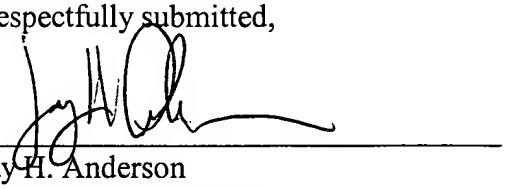
Accordingly, it is believed that the circuit of Claim 7 is clearly different from the circuit of Koch, so that the invention defined in Claim 7 is not anticipated by the cited reference.

The other claims in this application are each dependent from one or the other of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable reconsideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,



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